R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

Applicants thank Examiner Rodriguez for the indications of allowable matter.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments and new claims may be found in the specification, for example, on page 3 lines 6-7, page 6 lines 14-16, page 7, line 20-21, page 9, lines 17-20, claims 8, 9, 12 and 19 and FIGS. 2, 3 and 5 as originally filed. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1, 4-10, 16, 17 and 20 under 35 U.S.C. §103(a) as being unpatentable over Abbott et al. '249 (hereafter Abbott) in view of Cheung et al. '498 (hereafter Cheung) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 2, 11 and 18 under 35 U.S.C. §103(a) as being unpatentable over Abbott in view of Cheung and Izumi et al. '673 (hereafter Izumi) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 14 and 15 under 35 U.S.C. §103(a) as being unpatentable over Abbott in view of Cheung and Yang '728 has been obviated by appropriate amendment and should be withdrawn.

The rejection of claim 3 under 35 U.S.C. §103(a) as being unpatentable over Abbott in view of Cheung and Shimoda '120 has been obviated by appropriate amendment and should be withdrawn.

Abbott concerns a disk drive using PRML class IV sampling data detection with digital adaptive equalization (Title). Cheung concerns an asynchronous track code encodement and detection for disk drive servo control system (Title). Izumi concerns a digital recording/reproduction apparatus including a digital equalizer circuit with open-loop control (Title). Yang concerns a hard disk having extended data region (Title). Shimoda concerns a record reproduction apparatus (Title).

Claim 1 provides (in part) a filter circuit configured as a three-tap filter to generate a track ID signal. In contrast, both Abbott and Cheung appear to be silent regarding three-tap filters generating track ID information. Therefore, Abbott and Cheung, alone or in combination, do not appear to teach or suggest a filter circuit configured as a three-tap filter to generate a track ID signal as presently claimed.

Claim 1 further provides a filter circuit configured to reject a DC offset error in a digital signal. Despite the assertion on page 2 of the Office Action, the text in column 36,

lines 52-65 of Abbott appears to be silent regarding the operation of a filter circuit. In particular, the cited text of Abbott reads:

> The use of a digital gain control loop (as well as the use of a digital timing control loop as previously described hereinabove) has a number of advantages. First, a gain (or timing) control loop controlled via digital samples is less sensitive to variations in temperature, power supply and component tolerances than is a strictly analog control loop. Second, loop compensation or bandwidth may be easily adjusted or varied simply by loading registers, or by switching between banks of registers for "on the fly" changes. This means that optimal loop compensation may be used during both acquisition and tracking modes. Finally, the digital loop filter eliminates errors otherwise due to bias and offset that may exist in an analog-only loop filter implementation.

Nowhere in the above text does Abbott discuss a filter circuit rejecting a DC offset error in a signal presented from a FLASH A/D 46. Therefore, *prima facie* obviousness has not been established for lack of evidence that Abbott and Cheung teach all of the claim limitations. Claims 16 and 17 provide language similar to claim 1 As such, the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Furthermore, clear and particular motivation to combine Abbott and Cheung has not been established. The asserted motivation on page 3 of the Office Action, "to remove noise and harmonic[s] that can cause PES and phase jitter (which i[s] known to an artisan of ordinary skill in the art to be DC offset errors.)" does not appear to be from Abbott, Cheung or knowledge generally available to one of ordinary skill in the art as required

by MPEP §2142. Therefore, *prima facie* obviousness has not been established. The Examiner is respectfully requested to (i) identify the source of the asserted motivation and (ii) provide evidence that PES and phase jitter are know to artisans of ordinary skill in the art as "DC offset errors".

Claim 2 provides the filter circuit is further configured to implement each tap multiplication coefficients as an integer. In contrast, each of Abbott, Cheung and Izumi appear to be silent regarding each filter generating track ID information implementing integer tap coefficients. Therefore, Abbott, Cheung and Izumi, alone or in combination, do not appear to teach or suggest a filter circuit configured to implement each tap multiplication coefficients as an integer as presently claimed. Claim 18 provides language similar to claim 2. As such, claims 2 and 18 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 8 provides a magneto-resistive head asymmetry correction circuit coupled to a voltage gain circuit. Despite the assertion on page 4 of the Office Action, the text in column 9, lines 8-34 of Abbott appear to be silent regarding a magneto-resistive head asymmetry correction circuit. The cited text of Abbott reads:

> The heads 16 are positioned in unison with each movement of the actuator and head stack assembly 20, and the resulting vertically aligned, circular data track locations are frequently referred to as "cylinders" in the disk drive art.

> The storage disk may be an aluminum alloy or glass disk which has been e.g. sputter-deposited with a suitable multi-layer magnetic thin film and a protecting carbon overcoat in conventional fashion, for example. Other disks and magnetic media may be employed, including plated media and or spin-coated oxide media, as has been conventional in drives having lower data storage capacities and prime costs.
>
> A head select/read channel preamplifier 28 is preferably included within the HDA 12 in close proximity to the thin film heads 26 to reduce noise pickup. As is conventional, the preamplifier 28 is preferably mounted to, and connected by, a thin flexible plastic printed circuit substrate. A portion of the flexible plastic substrate extends exteriorly of the HDA 12 to provide electrical signal connections with the circuitry carried on the PCB 14. Alternatively, and equally preferably, the preamplifier 28 may be connected to the other circuitry illustrated in FIG. 4 exteriorly of the HDA 12 in an arrangement as described in the referenced copending U.S. patent application Ser. No. 07/881,678, filed on May 12, 1992, and entitled "Hard Disk Drive Architecture".

Nowhere in the above text, or in any other section, does Abbott appear to discuss a magneto-resistive head asymmetry correction circuit. Therefore, Abbott and Cheung, alone or in combination, do not appear to teach or suggest a magneto-resistive head asymmetry correction circuit coupled to a voltage gain circuit as presently claimed. As such, claim 8 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 9 provides both (i) a digital filter circuit configured to generate a filtered track ID signal and (ii) a position error signal filter configured to generate a filtered PES signal in response to the digital signal. In contrast, Cheung appears to contemplate a structure having a signal filter for both track information and position errors. In particular, column 5, lines 35-46 of Cheung reads:

> Thus, the demodulator preferably includes a squarer and finite impulse response filter with filter coefficients chosen to provide a harmonic notch Hilbert Transform filter function. In particular, some high density disk drives use read/write heads with magneto-resistive (MR) heads that produce second-order harmonics that the Hilbert Transform filter can effectively remove. **The filter also can be tailored to remove other noise and harmonic contents that can cause PES and track code conversion errors** due to sampling clock error and phase jitter. (Emphasis added)

Cheung appears to implement a single filter whereas the claim provides two filters. Therefore, Abbott and Cheung, alone or in combination, do not appear to teach or suggest both (i) a digital filter circuit configured to generate a filtered track ID signal and (ii) a position error signal filter configured to generate a filtered PES signal in response to the digital signal as presently claimed. As such, claim 9 is fully patentable over the cited references and the rejection should be withdrawn.

Claims 3-7, 10, 11, 14, 15 and 20 depended either directly or indirectly from independent claims 1 or 17, which are now believed to be allowable. As such, the presently pending invention is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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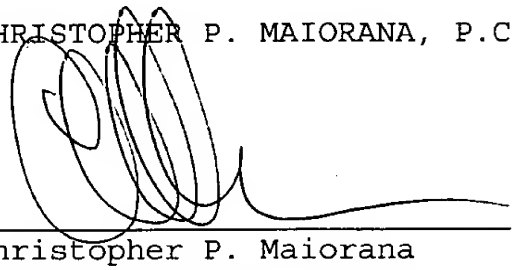

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